AMENDMENTS TO THE CLAIMS

Please cancel claims 1-5 without prejudice.

Claims 1-5 (cancelled)

Claim 6 (currently amended): A semiconductor memory device, comprising:

~~a charging circuit according to claim 1;~~

a charging driving circuit connected to the load circuit for supplying a charging signal to the load circuit from an output end of the charging driving circuit;

a time constant circuit for receiving the charging signal, changing a time constant of the charging signal and outputting a transition signal having a prescribed transition time period;

a control circuit for outputting a control signal for setting a time constant of the time constant circuit in accordance with the prescribed load circuit;

a voltage detection circuit for detecting that the transition signal output from the time constant circuit has reached the prescribed potential and outputting a detection signal; and

a delay and inversion circuit for delaying, and inverting a logic level of , an externally input charging control signal, and outputting a delay signal,

wherein the charging driving circuit starts a charging operation in accordance with the delay signal output from the delay and inversion circuit, and terminates the charging operation in accordance with the detection signal output from the voltage detection circuit;

a pair of complementary bit lines connected to a memory cell; and

an equalizing circuit for equalizing the pair of complementary bit lines to an equal prescribed potential using an equalizing signal acting as a charging control signal,

wherein an output end of the charging driving circuit of the charging circuit is connected to the pair of complementary bit lines.

Claim 7 (original): A semiconductor memory device according to claim 6, comprising at least one more pair of complementary bit lines, wherein the output end of the charging driving circuit of the charging circuit is connected to the pairs of complementary bit lines.

Claim 8 (original): A semiconductor memory device according to claim 6, wherein the equalizing circuit includes a pull-up circuit for charging the pair of complementary bit lines to a prescribed potential.

Claim 9 (original): A semiconductor memory device according to claim 6, wherein the equalizing circuit includes a pull-up circuit for charging the pair of complementary bit lines to a prescribed potential, and the delay and inversion circuit of the charging circuit provides a delay time period which is at least equal to a time period required for the pair of complementary bit lines, charged to the prescribed potential by the pull-up circuit, to be discharged via the output end of the charging driving circuit.

Claim 10 (original): A semiconductor memory device according to claim 8, wherein the delay and inversion circuit of the charging circuit provides a delay time period which is at least equal to a time period required for the pair of complementary bit lines, charged to the prescribed potential by the pull-up circuit, to be discharged via the output end of the charging driving circuit.